AN-6067

Design and Application of Primary-Side Regulation (PSR) PWM Controller

FAN100 / FAN102 / FSEZ1016A / FSEZ1216

Abstract

This application note describes a typical charger using the PSR controller. Both the features of this controller, as well as the operation of the power supply adaptor, are presented in detail. Based on the proposed design guideline, a design example with detailed parameters is given to demonstrate the superior performance of the controller.

Applications

- Battery chargers for cellular phones, cordless phones, PDAs, digital cameras, power tools
- Optimal choice for the replacement of linear transformers and RCC SMPS

Features

- Constant-Voltage (CV) and Constant-Current (CC) Control without Secondary-Feedback Circuitry
- Accurate Constant Current Achieved by Fairchild's Proprietary *TRUECURRENT*™ Technique
- Green-Mode Function: PWM Frequency Decreasing Linearly
- Fixed PWM Frequency at 42kHz with Frequency Hopping to Solve EMI Problems
- Low Startup Current: 10μA (Typical)
- Low Operating Current: 3.5mA (Typical)
- Peak-Current-Mode Control
- Cycle-by-Cycle Current Limiting
- V_{DD} Over-Voltage Protection (OVP)
- V_{DD} Under-Voltage lockout (UVLO)
- Gate Output Maximum Voltage Clamped at 18V
- Fixed Over-Temperature Protection (OTP)
- Cable Compensation for Tight CV Regulation (FAN102 / FSEZ1216)

PSR PWM Controller

FAN100	PSR PWM Controller
FAN102	FAN100 + Cable Compensation
FSEZ1016A	FAN100 + MOSFET (1A/600V)
FSEZ1216	FAN102 + MOSFET (1A/600V)

Pin Configurations

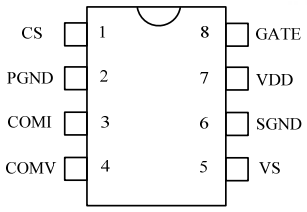

Figure 1. FAN100

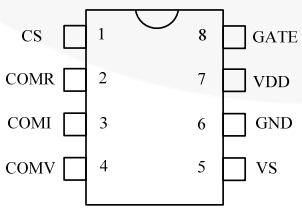

Figure 2. FAN102

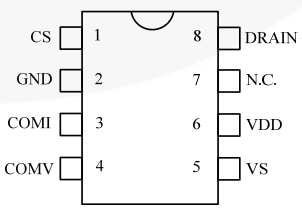

Figure 3. FSEZ1016A

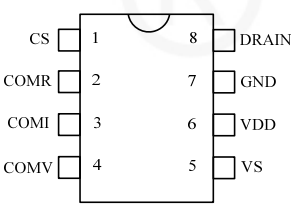

Figure 4. FSEZ1216

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Typical Applications

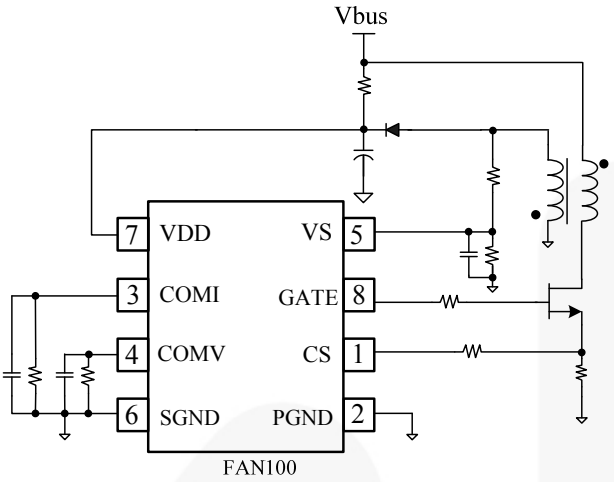

Figure 5. FAN100

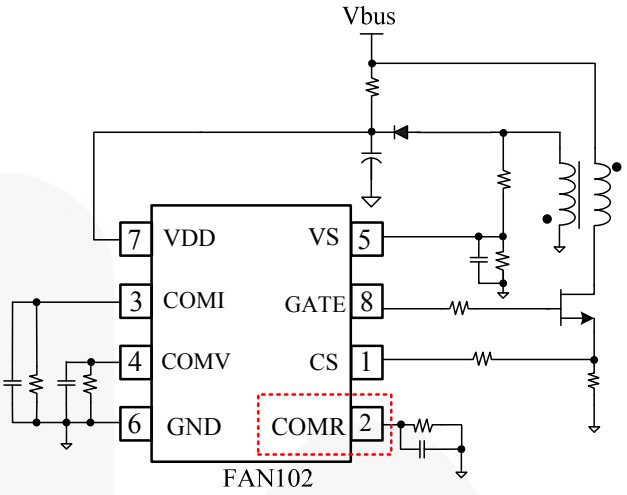

Figure 6. FAN102 (FAN100 + Cable Compensation)

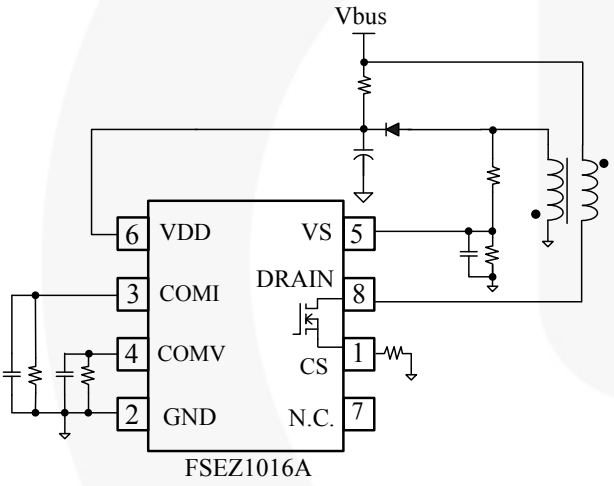

Figure 7. FSEZ1016A (FAN100 + MOSFET)

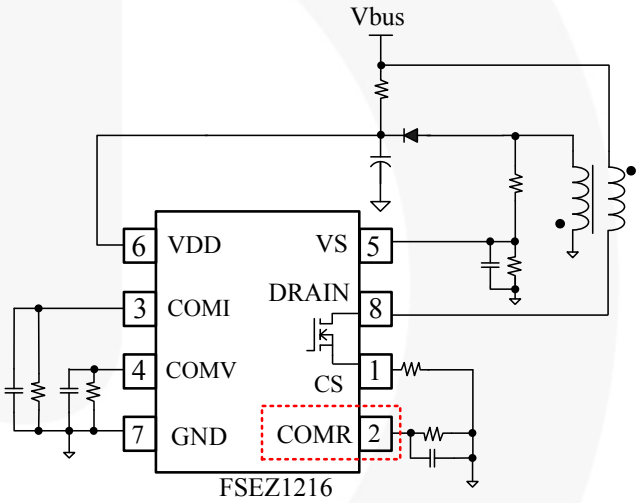

Figure 8. FSEZ1216 (FAN102 + MOSEFET)

Block Diagrams

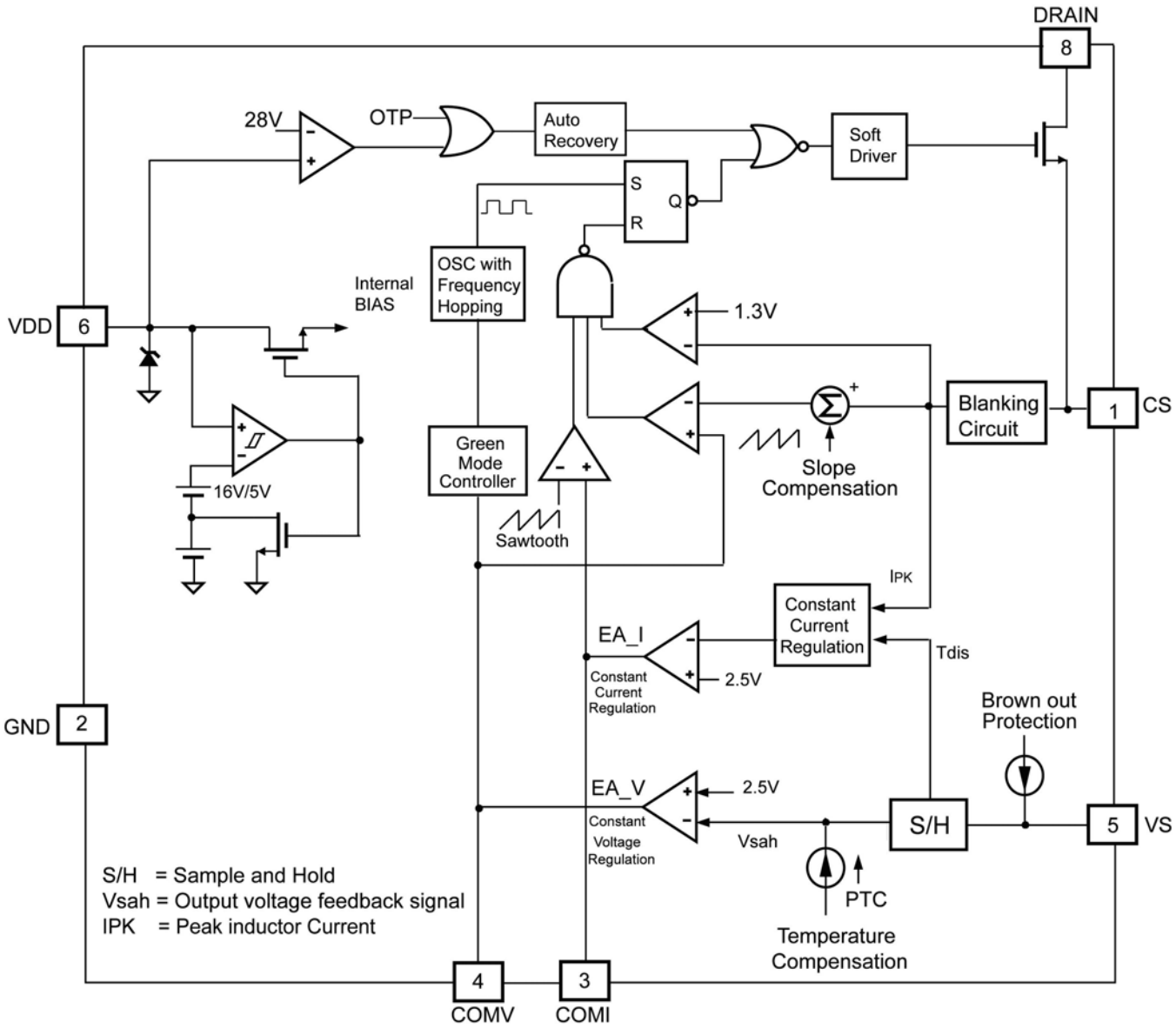

Figure 9. FSEZ1016A (FAN100 + MOSFET)

Block Diagrams (Continued)

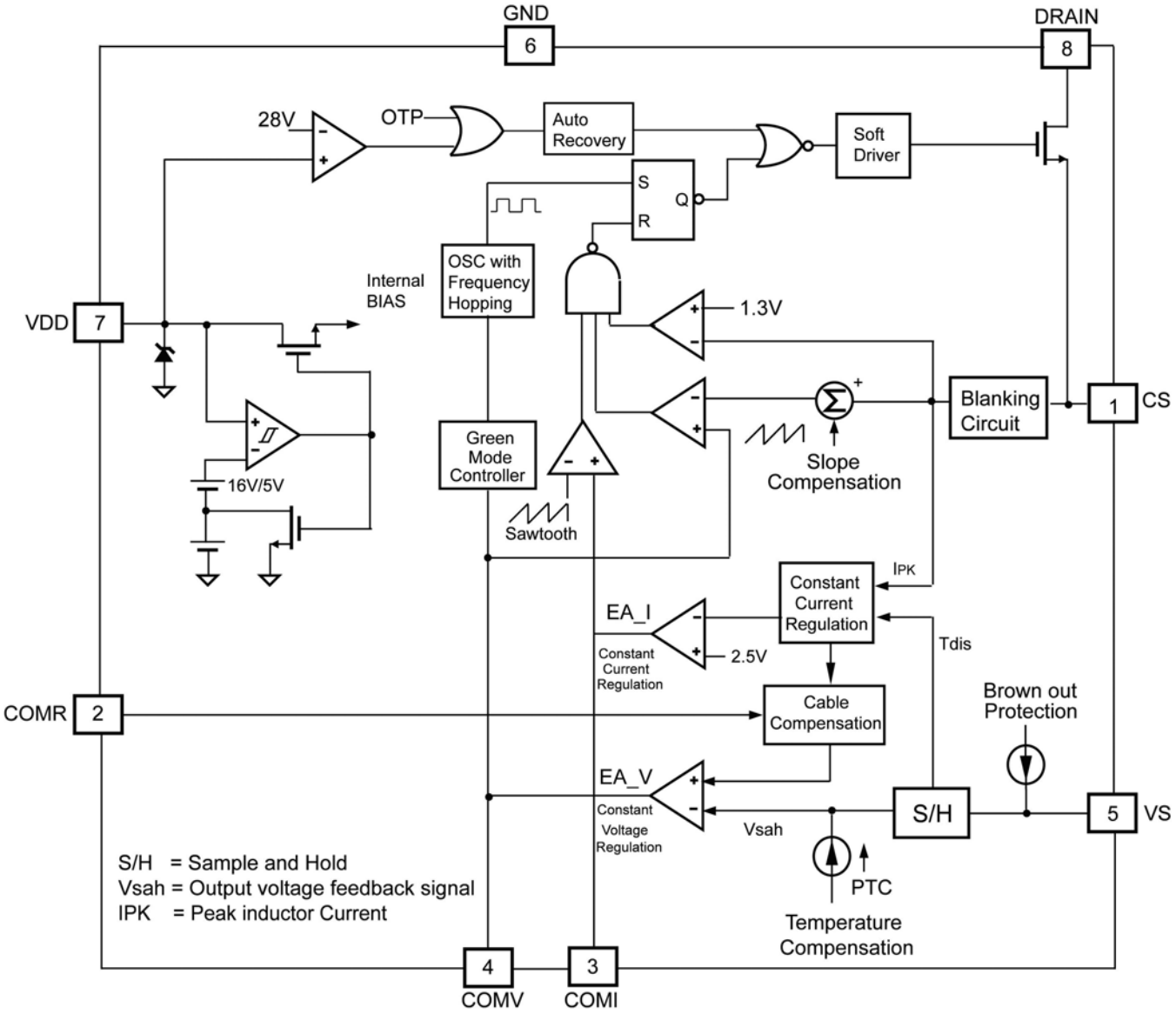

Figure 10. FSEZ1216 (FAN102 + MOSFET)

Introduction

This highly integrated PSR PWM controller contains several features to enhance the performance of low-power flyback converters. The patented topology of the PSR controller allows for simplified of circuit designs, particularly battery charger applications. CV and CC control can be accurately achieved without secondary feedback circuitry. With the addition of frequency-hopping in PWM operation, EMI problems can be solved using minimized filter components. As a result, a low-cost, smaller, and lighter charger is produced when compared to a conventional design or a linear transformer.

To minimize standby power consumption, the proprietary green-mode function provides off-time modulation to linearly decrease the PWM frequency under light-load conditions. This green-mode function is designed to help the power supply meet power conservation requirements. The startup current is only 10μA, which allows for the use of large startup resistance for further power savings.

The PSR controller also provides numerous protection functions. The VDD pin is equipped with over-voltage protection and under-voltage lockout. Pulse-by-pulse current limiting and CC control ensure over-current protection during heavy loads. The GATE output is clamped at 15V to protect the external/internal MOSFET from over-voltage damage. Additionally, the internal over-temperature-protection function shuts down the controller with auto recovery when over heating occurs.

By using the PSR controller, a charger can be implemented with few external components and at a minimized cost.

Internal Block Operation

Constant Voltage Output Regulation

PSR controller's innovative method can achieve accurate output CV/CC characteristic without voltage and current sensing circuitry on the secondary side. The application circuit and a conceptualized internal block diagram relating to the constant voltage regulation are shown in Figure 11, and the key waveform is shown in Figure 12. The secondary output status is taken from the primary auxiliary winding when the MOSFET is off. A unique sampling method is used to acquire a duplication of the output voltage (V_{sah}) and the output diode discharge time (t_{dis}). The sampled voltage (V_{sah}) is then compared with the precise internal reference voltage (V_{ref}) to determine the on-time of the MOSFET by modulating error amplifier's output. This inexpensive method achieves accurate output voltage regulation.

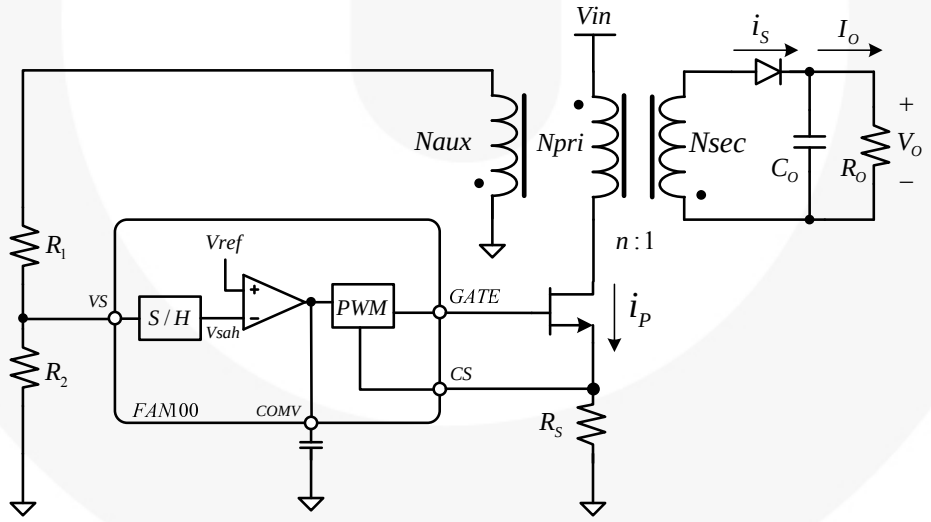

Figure 11. Internal Block of Constant Voltage Output Operation

Constant Current Output Regulation

As shown in Figure 12, the output current I_O can be expressed by Equation 1 when the flyback converter is operated in DCM. As a result, the output current I_O can be calculated by the signal i_{pk}, t_{dis}. The PSR controller then determines the on-time of the MOSFET to modulate input power and provide constant output current.

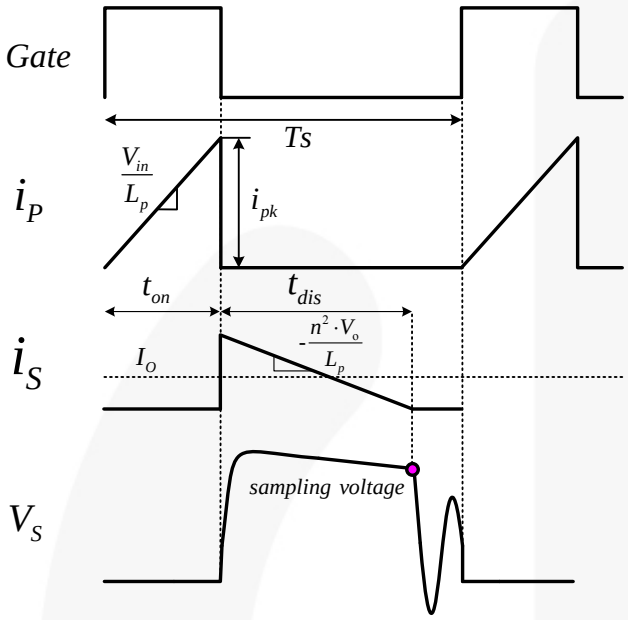

Figure 12. Principal Operation Waveform of the Flyback Converter (DCM)

The current-sense resistor can adjust the value of the constant current. Through better design of the transformer operations under discontinuous current mode, the PSR controller's proprietary control structure is able to achieve accurate and constant current characteristics. Detailed design guideline for the transformer is introduced in the following section.

$$Io = \frac{1}{2Ts} \cdot \left[t_{dis} \cdot i_{s,pk} \right] = \frac{1}{2Ts} \cdot \left[n_p \cdot i_{pk} \cdot t_{dis} \right] = \frac{1}{2Ts} \cdot \left[n_p \cdot \frac{V_{CS}}{R_{CS}} \cdot t_{dis} \right] \quad (1)$$

where:

$i_{s,pk}$ is the peak inductor current of the secondary side,

i_{pk} is the peak inductor of primary side.

t_{dis} is discharge-time of transformer inductor current.

n_p is the turn ratio between primary and secondary winding.

R_{CS} is the current-sense resistor.

V_{CS} is the voltage on current-sense resistor.

Green-Mode Operation

The proprietary green-mode function of the PSR controller provides off-time modulation to linearly decrease the PWM frequency at light-load conditions, as low as 500Hz. With the green-mode function, the power supply can easily meet the most stringent of power conservation requirements.

Figure 13 shows the characteristics of the PWM frequency vs. the output voltage of the error amplifier (V_{COMV}). The PSR controller uses the positive, proportional, output load parameter (V_{COMV}) as an indication of the output load for modulating the PWM frequency. In heavy load conditions, the PWM frequency is fixed at 42KHz. Once V_{COMV} is lower than V_N, the PWM frequency starts to linearly decrease from 42KHz to 500Hz. Figure 14 is a measured waveform at burst-mode operation.

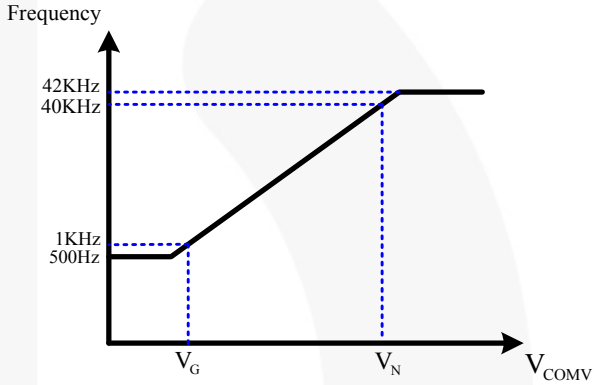

Figure 13. PWM Frequency vs. V_{COMV}

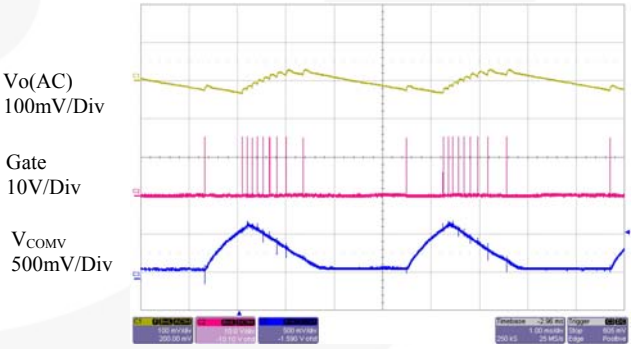

Figure 14. Measured Waveform at Burst-Mode Operation

Frequency Hopping Operation

A frequency hopping function is built in to further improve EMI system performance. The frequency hopping period is no longer than 3ms and the PWM switching frequency range is 42kHz +/- 2.6kHz.

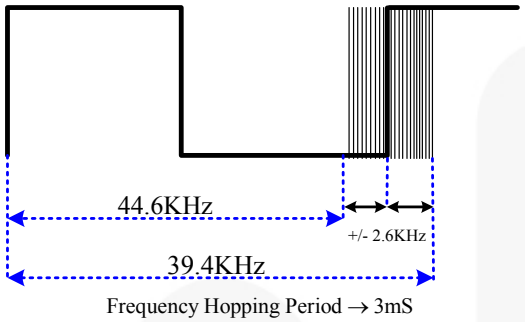

Figure 15. Gate Signal with Frequency Hopping

CV / CC Regulation

Battery chargers are typically designed for two modes of operation, constant-voltage charging and constant-current charging. The basic charging characteristic is shown in Figure 16. When the battery voltage is low, the charger operates on a constant current charging. This is the main method for charging batteries and most of the charging energy is transferred into the batteries. When the battery voltage reaches its end-of-charge voltage, the current begins to taper-off. The charger then enters the constant voltage method of charging. Finally, the charging current continues to taper-off until reaching zero.

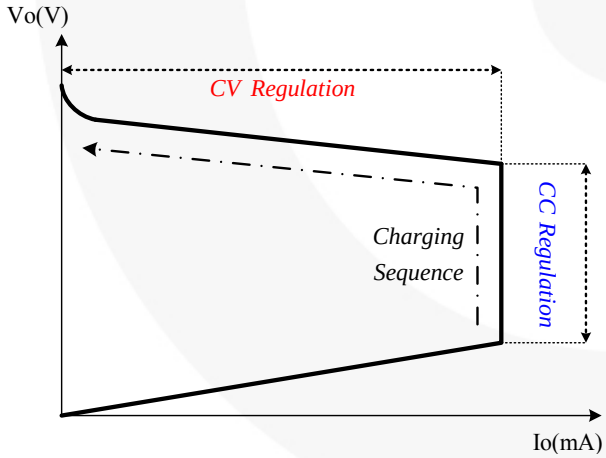

Figure 16. Basic Charging V-I Characteristic

As mentioned in the CV regulation region section, the V_{COMV} modulates MOSFET's on-time and PWM frequency to provide enough power to the output load. As shown in Figure 17, as the output load increases, V_{COMV} gradually rises until the system shifts into the CC regulation region. At the same time, V_{COMV} increases to 4.5V and the MOSEFT's on time is controlled by V_{COMI}. However, when power system operates in the CC regulation region at a fixed 42kHz frequency, the MOSFET's on-time is determined by V_{COMI} to modulate the output current.

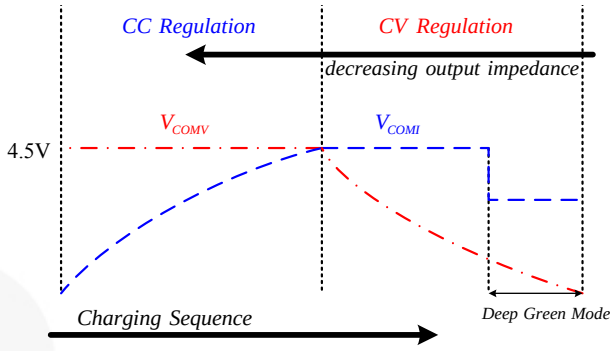

Figure 17. CV/CC Regulation Charging Sequence

Temperature Compensation

The PSR controller has built-in temperature compensation circuitry to provide constant reliable voltage regulation even at a different ambient temperature. This internal positive temperature coefficient (PTC) compensation current is used to compensate for the temperature due to the forward-voltage drop of the diode output. Without temperature compensation, the output voltage is distinctly higher in high temperatures than in lower temperature condition, as shown in Figure 18.

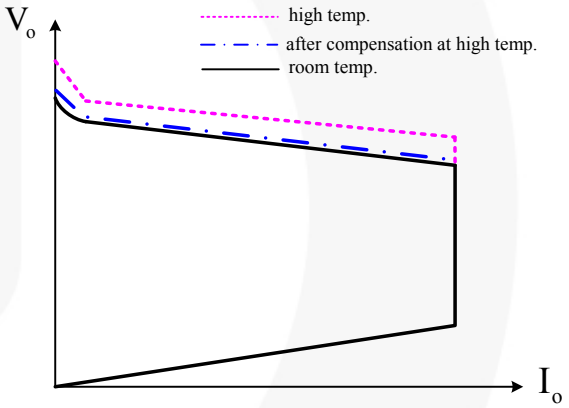

Figure 18. Output V-I Curve with Temperature Compensation

As shown in Figure 19, the accuracy value of R1 and R2 determines the voltage regulation amount. The suggested deviation for R1 and R2 is a +/-1% tolerance.

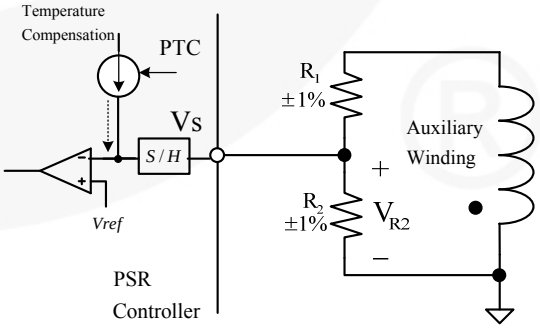

Figure 19. Temperature Compensation

Startup Circuitry

When the power is activated, the input voltage charges the hold-up capacitor (C1) via the startup resistors, as shown in

Figure 20. As the voltage (V_{DD}) reaches the startup voltage threshold (V_{DD-ON}), the PSR controller activates and drives the entire power supply.

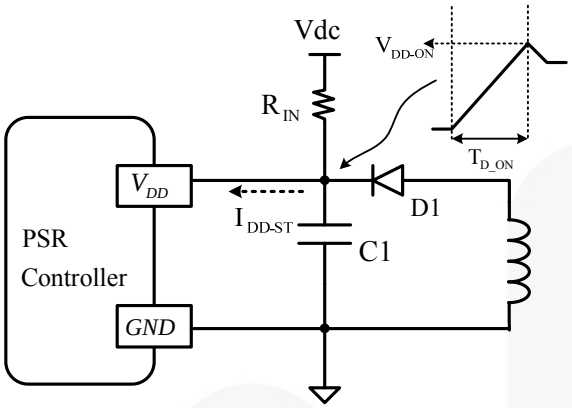

Figure 20. Single-Step Circuit Connected to the PSR Controller

The power-on delay is determined as follows:

$$T_{D_ON} = -R_{IN} \cdot C_1 \cdot \ln\left(1 - \frac{V_{DD-ON}}{V_{ac} \cdot \sqrt{2} - I_{DD-ST} \cdot R_{IN}}\right) \quad (2)$$

where I_{DD-ST} is the startup current of the PSR controller.

Due to the low startup current, a large R_{IN} value, such as 1.5MΩ can be used. With a hold-up capacitor of 4.7μF, the power-on delay T_{D_ON} is less than 3s for a $90V_{AC}$ input.

If a shorter startup time is required, a two-step startup circuit, as shown in Figure 21, is recommended. In this circuit, a smaller C1 capacitor can be used to decrease startup time without a need for a smaller startup resistor (R_{IN}) and increase the power dissipation on the R_{IN} resistor. The energy supporting the PSR controller after startup is mainly from a larger capacitor C2.

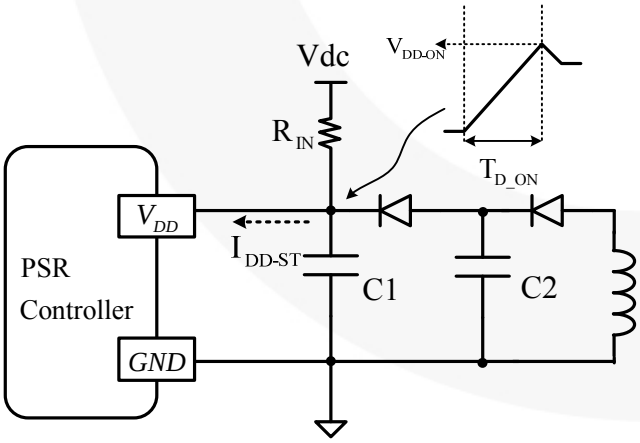

Figure 21. Two Steps of Providing Power to the PSR Controller

The maximum power dissipation of R_{IN} is:

$$P_{R_{IN},MAX} = \frac{\left(V_{dc,\max} - V_{DD}\right)^2}{R_{IN}} \cong \frac{V_{dc,\max}^{\ 2}}{R_{IN}} \quad (3)$$

where $V_{dc,max}$ is the maximum rectified input voltage.

Take a wide-ranging input ($90V_{AC}$~$264V_{AC}$) as an example, V_{dc} =100V~380V:

$$P_{R_{IN},MAX} = \frac{380^2}{1.5 \times 10^6} \cong 96mW \quad (4)$$

Built-in Slope Compensation

The sensed voltage across the current sense resistor is used for peak-current-mode control and cycle-by-cycle current limiting. Within every switching cycle, the PSR controller produces a positively sloped, synchronized ramp signal. The built-in slope compensation function improves power supply stability and prevents peak-current-mode control from causing sub-harmonic oscillations.

Leading Edge Blanking (LEB)

Each time the MOSFET is powered on, a spike, induced by the diode reverse recovery and by the output capacitances of the MOSFET and diode, appears on the sensed signal. To avoid premature termination of the MOSEFT, a leading-edge blanking time is introduced in the PSR controller. During the blanking period, the current-limit comparator is disabled and unable to switch off the gate driver.

Under-Voltage Lockout (UVLO)

The power-on and off thresholds of the PSR controller are fixed at 16V/5V. During startup, the hold-up capacitor must be charged to 16V through the startup resistor to enable PSR controller. The hold-up capacitor continues to supply V_{DD} until power can be delivered from the auxiliary winding of the main transformer (V_{DD} must not drop below 5V during this startup process). This UVLO hysteresis window ensures that the hold-up capacitor can adequately supply V_{DD} during startup.

V_{DD} Over-Voltage Protection (OVP)

V_{DD} over-voltage protection prevents damage due to over-voltage conditions. When V_{DD} exceeds 28V due to abnormal conditions, PWM output is turned off. Over-voltage conditions are usually caused by open feedback loops.

Over-Temperature Protection (OTP)

The PSR controller has a built-in temperature sensing circuit to shut down the PWM output if the junction temperature exceeds 145°C. When the PWM output shuts down, the V_{DD} voltage gradually drops to the UVLO voltage. Some of the internal circuits shut down and V_{DD}

gradually starts increasing again. When V_{DD} reaches 16V, all the internal circuits, including the temperature sensing circuit, start operating normally. If the junction temperature is still higher than 145°C, the PWM controller shuts down immediately. This continues until the temperature drops below 120°C.

GATE Output

The PSR controller BiCMOS output stage is a fast totem pole gate driver. Cross conduction design elimination was used to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped by an internal 15V Zener diode for the protection of power MOSFET against over-voltage gate signals.

Brownout Protection

The PSR controller has a built-in brownout protection circuit to shut down the PWM output. As the input voltage decreases, the flowing current from VS pin is less than I_{VS-UVP}, the PWM output shuts down immediately and enters an auto restart mode. The V_{DD} voltage gradually drops to the UVLO voltage.

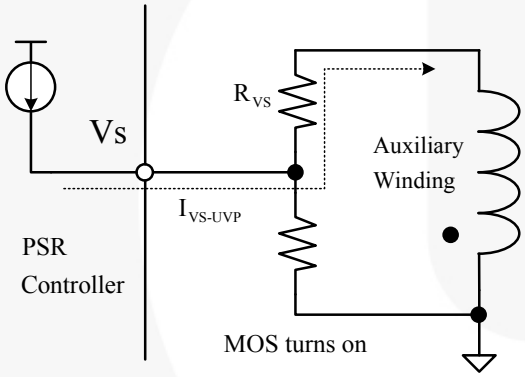

Figure 22. Brownout Protection

Cable Compensation

The FAN102/FSEZ1216 PWM controller has a cable compensation function used to compensate the output voltage drop due to output cable loss. Use an external resistor connected from COMR pin to GND adjusts the amount of cable compensation.

In CV regulation control, the on-time of MOSFET only regulates on-board voltage, not including output cable. Different cable wire gauge or length results in different output voltage. As previous mentioned in the CC regulation control section that can calculate the output current. This calculated signal can provide the controller the output load condition and determine the amount of cable compensation, then rescue output voltage drop. To calculate compensation percentage, use the equation below:

$$R_{COMR} = \frac{Percentage}{100.8 \times 10^{-6}} \quad (5)$$

For example, a power board for a charger application is 5V/1A. Short the COMR pin to GND first and measure the output voltage from light load to maximum load. If the output voltage with cable is 4.7V at 1A, the percentage to 5V is 6%. Calculate the R_{COMR} as:

$$R_{COMR} = \frac{6}{100.8 \times 10^{-6}} \cong 59.5K\Omega \quad (6)$$

Choose the approximate value of R_{COMR} and let the output voltage compensate gradually. Figure 23 is R_{COMR} compared to percentage curve for reference.

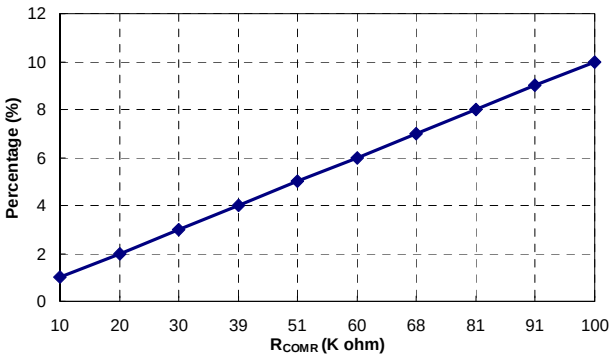

Figure 23. R_{COMR} vs. Percentage

Lab Note

Before reworking or soldering / desoldering on the power supply, **discharge the primary capacitors by way of the external bleeding resistor**. If not, the PWM IC may be destroyed by external high-voltage discharge during the soldering / desoldering.

Application Information

Transformer Design

The transformer inductor current must operate in DCM under any conditions. A typical output V-I curve is shown in Figure 24. For discontinuous current mode operation, the transformer inductor should be small enough to meet this condition. Point "B" is the lowest output voltage within the CC regulation and the widest discharge time of the transformer inductor due to the reflected voltage on the primary inductor. It is the easiest into CCM condition for transformer inductor.

Point "A" is the maximum output power of the power system. Ensure that the magnetic flux density falls within 0.25~0.3 Tesla, considered a safe range. The number of turns for primary transformer inductor can be determined on point "A." Figure 25 shows the characteristic curve of turn ratio and transformer inductance.

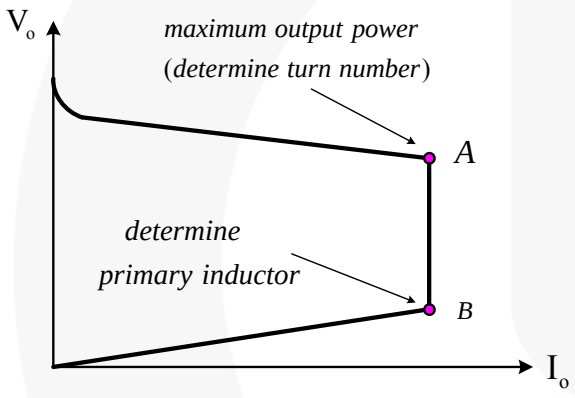

Figure 24. Critical Operating Points to Determine the Transformer

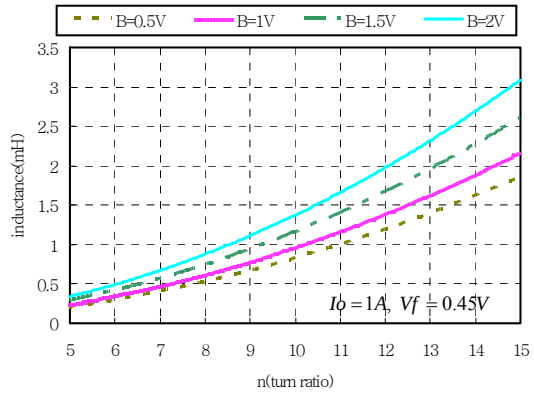

Figure 25. Characteristic Curve of Turn Ratio and Inductance

Determine Maximum and Minimum Input Voltage

Figure 26 shows the corrected input voltage waveform. The red line shows ripple voltage on the bulk capacitor and the minimum and maximum voltage on the bulk capacitor is expressed in equations 7 and 8, respectively. The C_{BULK} is the input capacitor and a typical value is 2-3µF per watt of output power for wide range input voltage (90-264V).

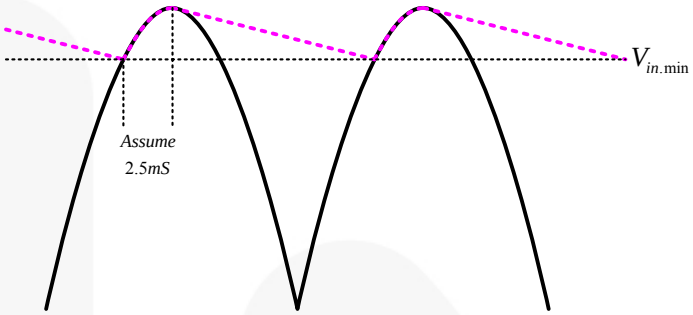

Figure 26. Bridge Rectifier and Bulk Capacitor Voltage Waveform

$$V_{in.\min} = \sqrt{2 \cdot V_{ac,\min}^{\ 2} - \frac{2 \cdot V_o \cdot I_o \cdot (1-0.3)}{\eta \cdot C_{bulk} \cdot 120}} \quad (7)$$

$$V_{in.\max} = \sqrt{2} \cdot V_{ac.\max} \quad (8)$$

Determine the Turn Ratio

The transformer turn ratio (n_p=N_{pri}/N_{sec}) is an important parameter of the flyback converter; it affects the maximum duty ratio when the input voltage is at a minimum value. It also influences the voltage stresses on the MOSFET and the secondary rectifier. The permissible voltage stresses and the maximum voltage stresses on the MOSFET, as well as the secondary rectifier, can be expressed as:

$$V_{DS.\max} = V_{in.\max} + n_p \cdot (V_o + V_f) \quad (9)$$

$$V_{F.\max} = \frac{V_{in.\max}}{n_p} + V_o \quad (10)$$

The leakage spike due to leakage inductance on the MOSFET and rectifier must also be taken into account.

Determine Transformer Inductance

Determine the V_{DD} voltage level and if the output voltage is defined. The turn ratio between auxiliary winding and secondary winding can be calculated as:

$$n_a = \frac{V_{DD} + V_{fa}}{V_O + V_f} \quad (11)$$

where V_{DD} is voltage on V_{DD} cap, usually ranging from about 15V~20V.

In the CC regulation region, on point "B," the power system shuts down if the output voltage is too low and the V_{DD}

voltage reaches the turn-off threshold voltage of the PSR controller. Therefore, if n_a was calculated, the $V_{O,"B"}$ can be obtained as:

$$V_{O,"B"} = \left(\frac{V_{fa} + 6.75 - V_f \cdot n_a}{n_a} \right) \quad (12)$$

where:

V_{fa} is forward-voltage of rectifier diode of auxiliary winding.

V_f is forward-voltage of output diode.

6.75V is typically the turn-off threshold voltage of the PSR controller.

The maximum duty ratio can be calculated by using a point "B" output condition:

$$d_{on.\max,"B"} = \frac{n_p \cdot (V_{o,"B"} + V_f)}{V_{in.\min,"B"} + n_p \cdot (V_{o,"B"} + V_f)} \quad (13)$$

The transformer inductance (L_p) is designed specifically for DCM operation and a CC tolerance of +/-10% should be considered. The transformer inductance can be obtained as:

$$L_p = \frac{\eta_{,"B"} \cdot V_{in.\min,"B"}^{\ 2} \cdot d_{\max,"B"}^{\ 2}}{2 \cdot V_{o,"B"} \cdot I_o \cdot f_s} \quad (14)$$

where:

$\eta_{,"B"}$ is the estimated system efficiency of point "B."

If no values are available, use 0.45~0.5 as an initial value.

f_s is the PWM frequency.

After the primary inductance is calculated, the maximum duty ratio of point "A" can be expressed as:

$$d_{on.\max,"A"} = \sqrt{\frac{2 \cdot V_{O,"A"} \cdot I_O \cdot L_P}{\eta_{,"A"} \cdot V_{in.\min,"A"}^{\ 2} \cdot T_s}} \quad (15)$$

where T_s is the switching period.

The primary peak inductor current (I_{PK}) of point "A" at full load and low line input voltage condition is:

$$i_{pk,"A"} = \frac{V_{in.\min,"A"}}{L_p} \cdot d_{on.\max,"A"} \cdot T_S \quad (16)$$

Determine Primary Inductance Turn Number

Based on Faraday's law and the peak inductor current, the minimum turns for the primary inductance is calculated as:

$$N_{pri} = \frac{L_p \cdot i_{pk,"A"}}{B_{\max} \cdot A_e} \cdot 10^6 \quad (17)$$

where:

B_{max} is the saturation magnetic flux density,

A_e is the effective area of the core-section.

The number of turns for the secondary winding is defined as:

$$N_{\sec} = \frac{N_{pri}}{n_p} \quad (18)$$

Once the secondary winding has been calculated, the number of turns for the auxiliary winding is defined as:

$$N_{aux} = n_a \cdot N_{\sec} \quad (19)$$

Determine the Divider Resistor (R_1) and Current-Sense Resistor (R_S)

Once the output voltage V_O and auxiliary winding have been defined, the feedback signal divider resistor, R_1, can be calculated as:

$$R_1 = R_2 \cdot \left[\frac{n_a}{V_{ref}} \cdot \left(V_O + V_f \right) - 1 \right] \quad (20)$$

where V_{ref}=2.5V, R_2 is typically set to 15~20KΩ.

As discussed in the *Constant Current Output Regulation* section, the region of constant current output operation can be adjusted by the current-sense resistor. After the turn ratio (n_p) has been determined, the relationship between the output current I_O and current sense resistor R_s is expressed as:

$$R_S = \frac{0.111875 \cdot n_p}{I_O} \quad (21)$$

As Figure 27 shows, a design spreadsheet can be used to calculate the transformer design and select the power system components for a first prototype. A 5V/1A design example is shown in Figure 27.

INPUT PARAMETER			SYSTEM PARAMETER			TRANSFORMER SPEC.		
Input Vac.min	90.000	V	V_O,"B"	1.808	V	Lp	1.683	mH
Input Vac.max	264.000	V	$V_{O(OVP)}$	8.247	V	Naux	32.578	T
Bulk Cap.	11.000	uF	V_{DD}	17.285	V	Npri	133.275	T
Output Voltage (A)-High	5.000	V	$V_{dc,max}$	373.296	V	Nsec	9.872	T
Output Current (A)	1.000	A	$V_{ds,max}$	446.871	V			
Output Voltage (B)-Low	5.000	V	$V_{F,max}$	32.652	V			
Output Current (B)	1.000	A	$V_{dc,min}$,"A"	91.659	V			
V_F	0.450	V	$D_{on.max}$,"A"	0.352				
V_{Fa}	0.700	V	I_{PK},"A"	0.456	A			
B_{max}	0.300	Tesla	$I_{SEC,PK}$,"A"	6.157	A			
Ae	19.200	mm^2	$I_{P,RMS}$,"A"	0.156	A			
Fs (Switching frequency)	42.000	KHz	$V_{dc,min}$,"B"	109.269	V			
Estimated Efficiency,"A"	0.680		$D_{on.max}$,"B"	0.218				
Estimated Efficiency,"B"	0.450		Ts	23.810	uS			
Np:Ns	13.500		R1(Divider Resistor)	123.880	K			
Na:Ns	3.300		T_{D_ON}(turn-on time)	2.306	S			
R2 (Divider Resistor)	20.000	K ohm	Rs(Current Sense Resistor)	1.510	ohm			
R_{IN}(Start-Up Resistor)	1500.000	K ohm						
V_{DD} Cap.	10.000	uF						

Figure 27. Calculated System Parameter by Design Spreadsheet

The parameters in Figure 27 can be found in the corresponding components in Figure 28.

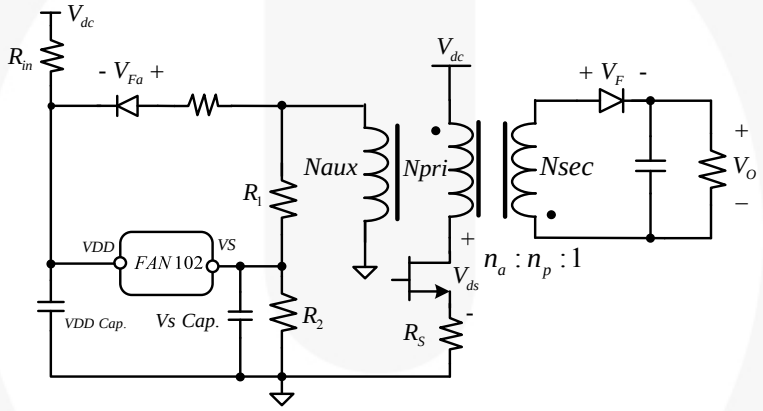

Figure 28. Application Circuit

Transformer Structure

As mentioned in the *Constant Voltage Output Regulation* section, the PSR controller incorporates a proprietary control design to achieve CV/CC regulations. A correct sampling voltage of the auxiliary winding is critical to the CV/CC performance. Therefore, the coupling of the auxiliary winding and the secondary winding should be precise. The suggested transformer structure is shown in Figure 29 and Figure 30. The coupling coefficient between the secondary winding and the auxiliary winding can be effectively improved by sloughing off the EMI shielding between auxiliary winding and secondary winding. Further effectiveness is achieved by increasing the coupling area through a well-paved the auxiliary winding on the top layer.

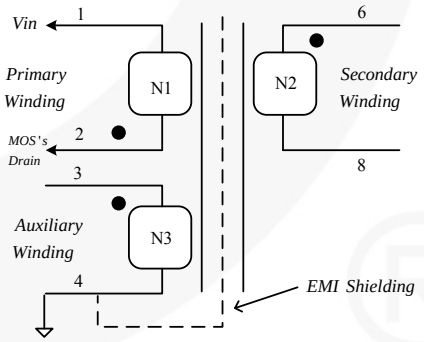

Figure 29. Transformer Winding

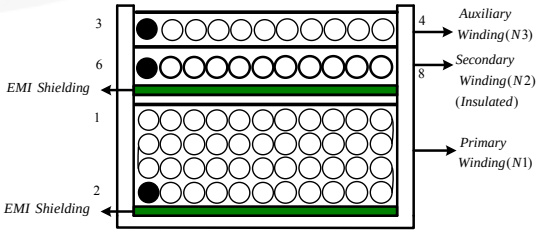

Figure 30. Recommended Transformer Structure

Effect of the Vs Pin Capacitor

A V_S capacitor with 22~68pF placed closely between Vs pin and the GND pin is recommended. The capacitor is used to bypass switching induced noise and keep the accuracy of the sampled voltage. The value of the capacitor affects the load regulation and constant current performance. Figure 31 illustrates the measured waveform on the Vs pin with a different V_S capacitor. If a higher value V_S capacitor is used, the charging time becomes longer and the sampled voltage is higher than the actual value. Figure 32 shows the effect on the sampled voltage with a different V_S capacitor.

Figure 33 shows a measured Vs pin waveform at a no-load condition. As illustrated, the feedback voltage is too narrow. Additionally, a large V_S capacitor causes the inaccurate sampling of the voltage; resulting in the rising of the output voltage. Figure 24 shows the influence of the V_S capacitor on the V-I curve.

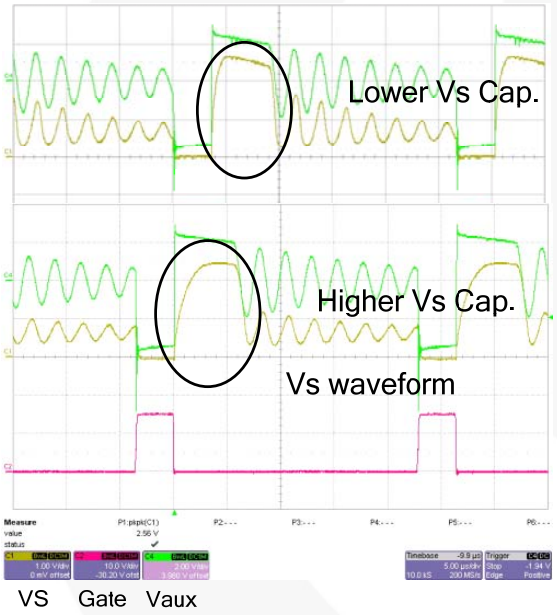

Figure 31. Measured Waveform with Different V_S Capacitor

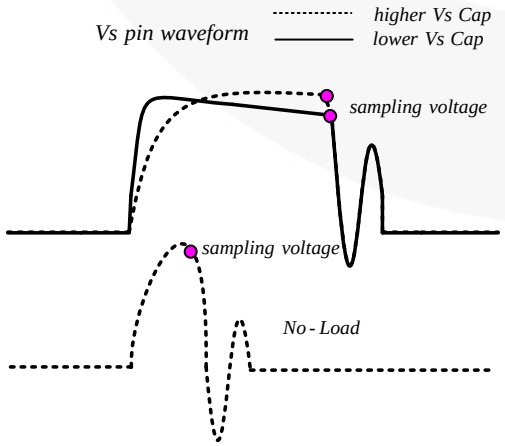

Figure 32. Effect on Sampling Voltage with Different V_S Capacitor

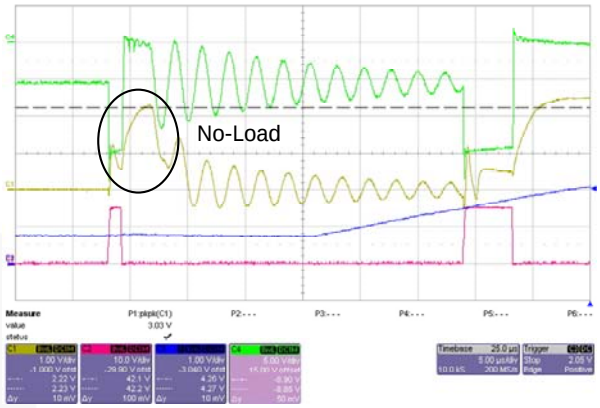

Figure 33. Measured Vs Pin Waveform at No Load

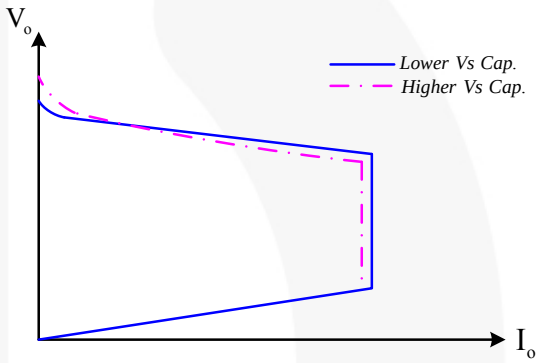

Figure 34. Comparison of V-I Curve with Different V_s Capacitor

Effect of V_{DD} and Snubber Capacitors

V_{DD} voltage and snubber capacitors are related to the feedback signal inaccuracy and cause output voltage to rise at no-load condition.

If the V_{DD} capacitor is not big enough, the decreasing PWM frequency at no-load condition causes V_{DD} voltage to drop quickly. In such a condition, the feedback signal is dominated by the V_{DD} voltage, but not the secondary output voltage. To avoid this, it is recommended the V_{DD} capacitor value be larger than 4.7µF(6.8~10µF).

On the other hand, the value of the snubber capacitor also affects the output voltage performance. When the MOSEFT is turned off, the polarity of the transformer primary side inductor is reversed and the energy stored in the transformer inductor is delivered to the secondary to supply load current. In the meantime, if the output voltage is higher than the voltage on the secondary winding (V_{sec}), the output diode is still reversed. The resulting voltage V_{pri} is then applied to the primary inductor, L_p, which charges the snubber capacitor. The charge time influences the feedback

voltage signal on the auxiliary winding. It is recommended that the snubber capacitor remain under 472pF(332~102pF).

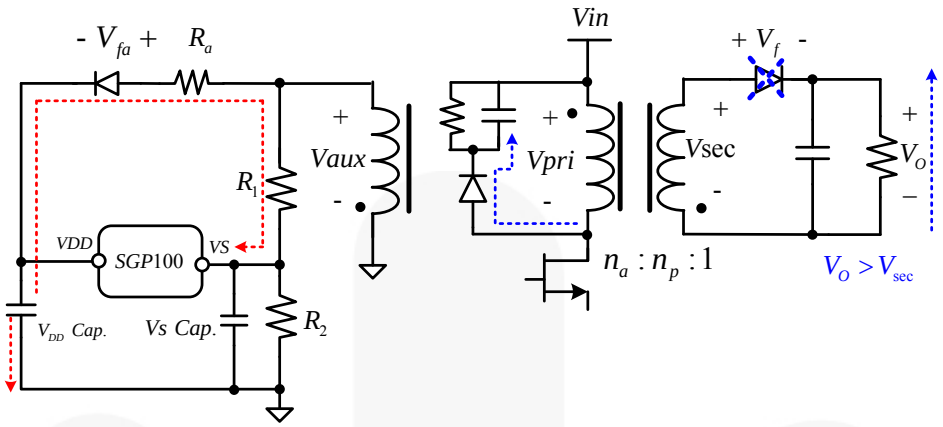

Figure 35. V_{DD} and Snubber Capacitors Effect on Output Voltage

Reducing No-Load Output Voltage with a "Dummy" Load

At no-load and very light load conditions, due to the very low PWM frequency caused by feedback signal deviations and output voltage rises, especially at low-line input voltage condition. Increasing the addition of a dummy load can fix this problem. Figure 36 shows the effect of a higher and lower dummy load on the V-I curve. The level of the dummy load is suggested at about 25~100mW.

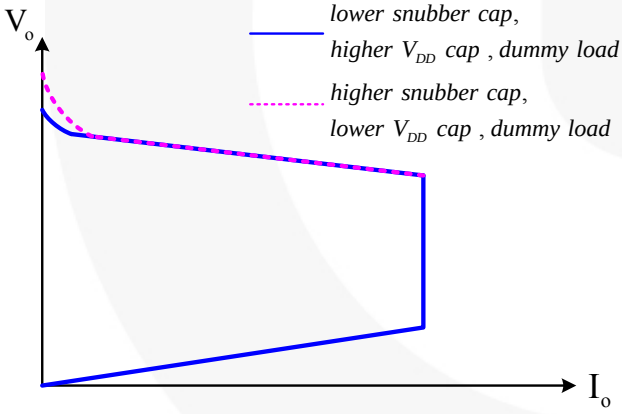

Figure 36. Dummy Load Effect on Output Characteristic

PCB Layout Considerations

High-frequency switching current / voltage make PCB layout a very important design issue. Good PCB layout minimizes excessive EMI and helps the power supply survive during surge/ESD tests.

General Guidelines

The numbers in the following guidelines refer to Figure 37.

To improve EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to capacitors C1 and C2 first, then to the switching circuits.

The high-frequency current loop is in **C2 – Transformer – MOSFET – R7 – C2**. The area enclosed by this current loop should be as small as possible.

Keep the traces (especially 4→**1**) short, direct, and wide. High voltage traces related to the drain of MOSFET and RCD snubber should be kept far way from control circuits to prevent unnecessary interference. If a heatsink is used for the MOSFET, connect this heatsink to a ground.

As indicated by **3**, the ground of the control circuits should be connected first, then to other circuitry.

As indicated by **2**, the area enclosed by the **transformer aux winding, D1 and C3**, should also be kept small.

Place C3 close to the PSR controller for good decoupling.

Suggestion for the Ground Connections

GND **3**→**2**→4→**1**: May make it possible to avoid common impedance interference for the sense signal.

Regarding the ESD discharge path, the charges go from secondary through the transformer stray capacitance to GND**2** first. Then the charges go from GND**2** to GND**1** and back to the mains. It should be noted that control circuits should not be placed on the discharge path.

5 Should a point-discharge route to bypass the static electricity energy. As shown in Figure 38, it is suggested to map out this discharge route.

Start in secondary GND to the **positive terminal of C2**, then to front terminal of bridge rectifier. If this discharge route is connected to the primary GND, it should be connected to the **negative terminal of C2 (GND1)** directly.

However, the creepage distance between these two pointed ends should be long enough to satisfy the requirements of applicable standards.

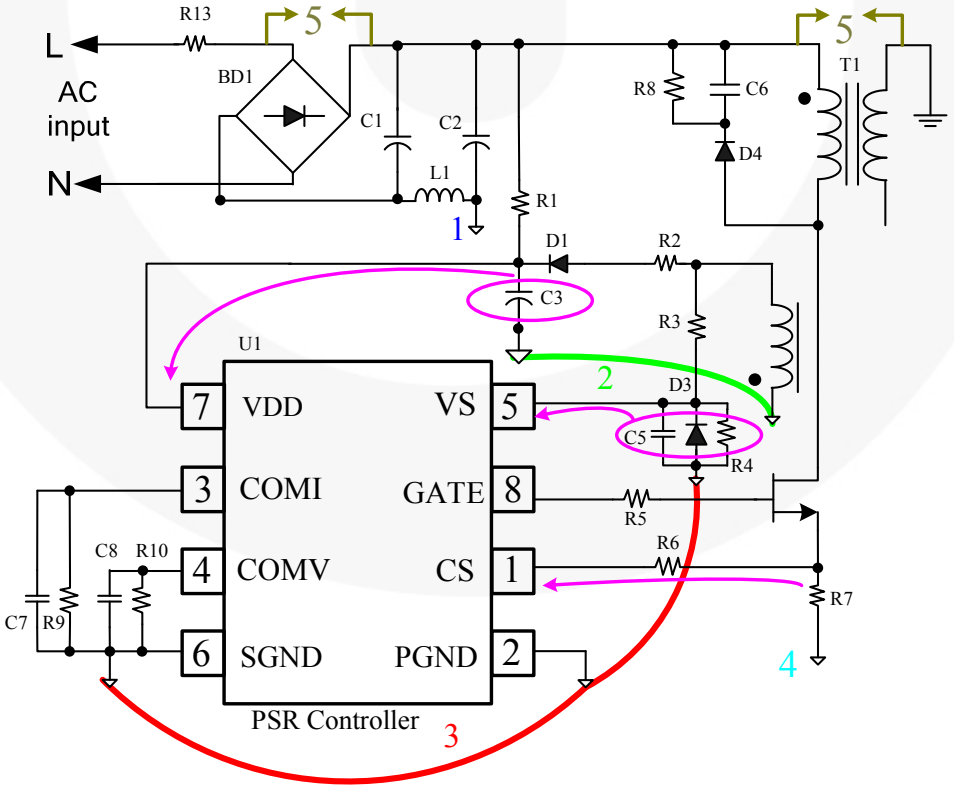

Figure 37. Layout Consideration

PCB Layout Considerations (Continued)

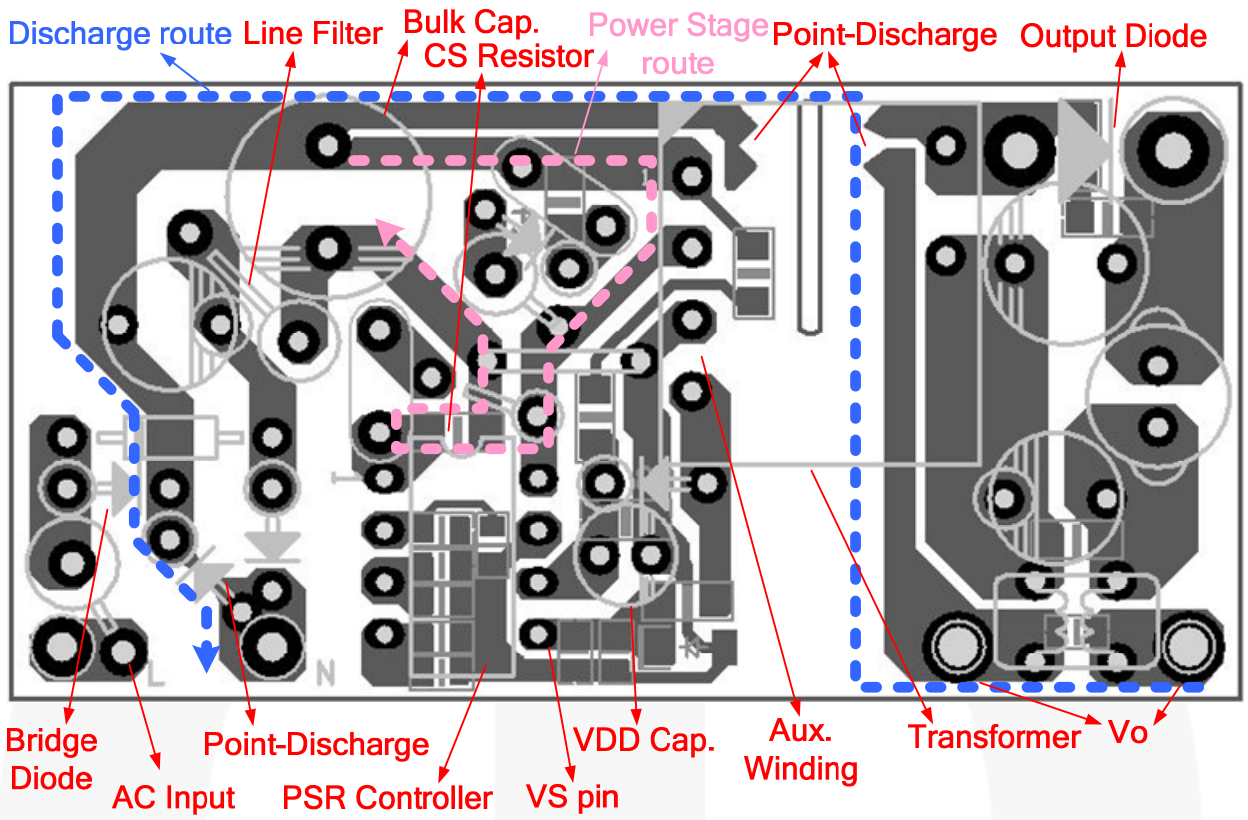

Figure 38. PCB Layout Example (5V/1A, 5W Power Board)

Reference Circuits

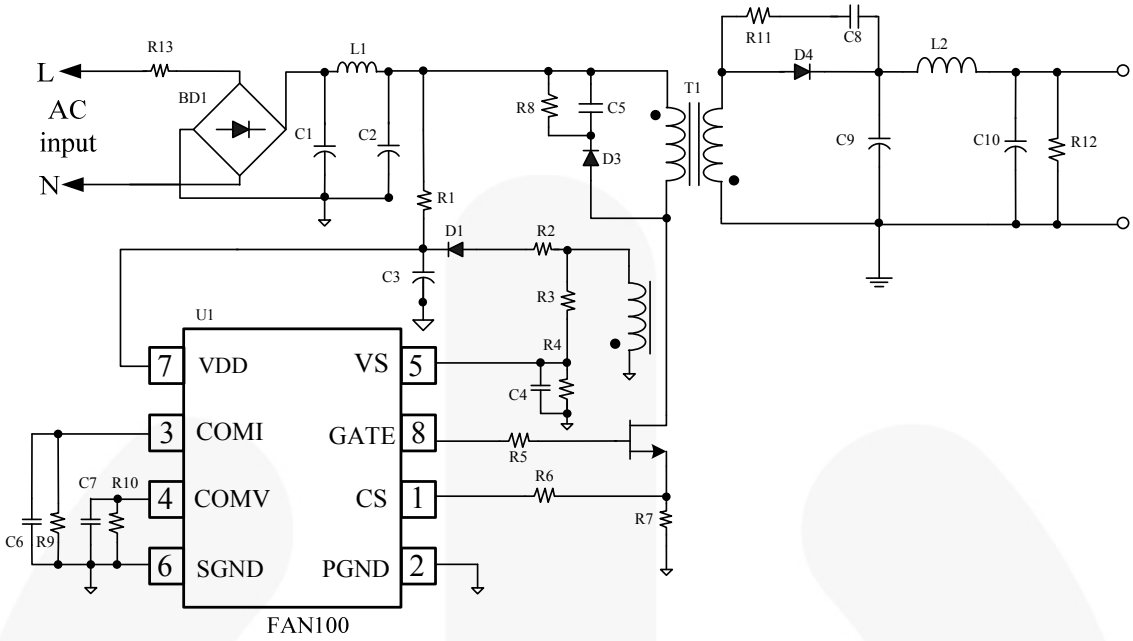

Figure 39. Application Circuit FAN100 (5V/1A)

BOM List

Symbol	Component	Symbol	Component
R1	Resistor 1.5MΩ 1/2W	D4	Diode 5A/60V SB560
R2	Resistor 4.7Ω	C1	Electrolytic Capacitor 1μF/400V
R3	Resistor 115KΩ 1%	C2	Electrolytic Capacitor 10μF/400V
R4	Resistor 18KΩ 1%	C3	Electrolytic Capacitor 10μF/50V
R5	Resistor 47Ω	C4	MLCC X7R 22pF
R6	Resistor 100Ω	C5	Snubber Capacitor 472pF/1KV
R7	Resistor 1.4Ω 1/2W 1%	C6	MLCC X7R 683pF
R8	Resistor 100KΩ 1/2W	C7	MLCC X7R 103pF
R9	Resistor 200KΩ	C8	MLCC 102pF/100V
R10	Resistor 30KΩ	C9	Electrolytic Capacitor 560uF/10V L-ESR
R11	Resistor 47Ω	C10	Electrolytic Capacitor 330μF/10V L-ESR
R12	Resistor 510Ω	L1	Inductor 1mH
R13	WireWound Resistor 18Ω	L2	Inductor 5μH
BD1	Rectifier Diode 1N4007 *4	Q1	Fairchild 2A/600V 2N60 TO-251
D1	Diode 1A/200V FR103	U1	FAN100
D3	Diode 1A/1000V 1N4007	TR1	EE-16 Lm=1.5mH Pri:Sec:Aux=135:10:33

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Reference Circuits (Continued)

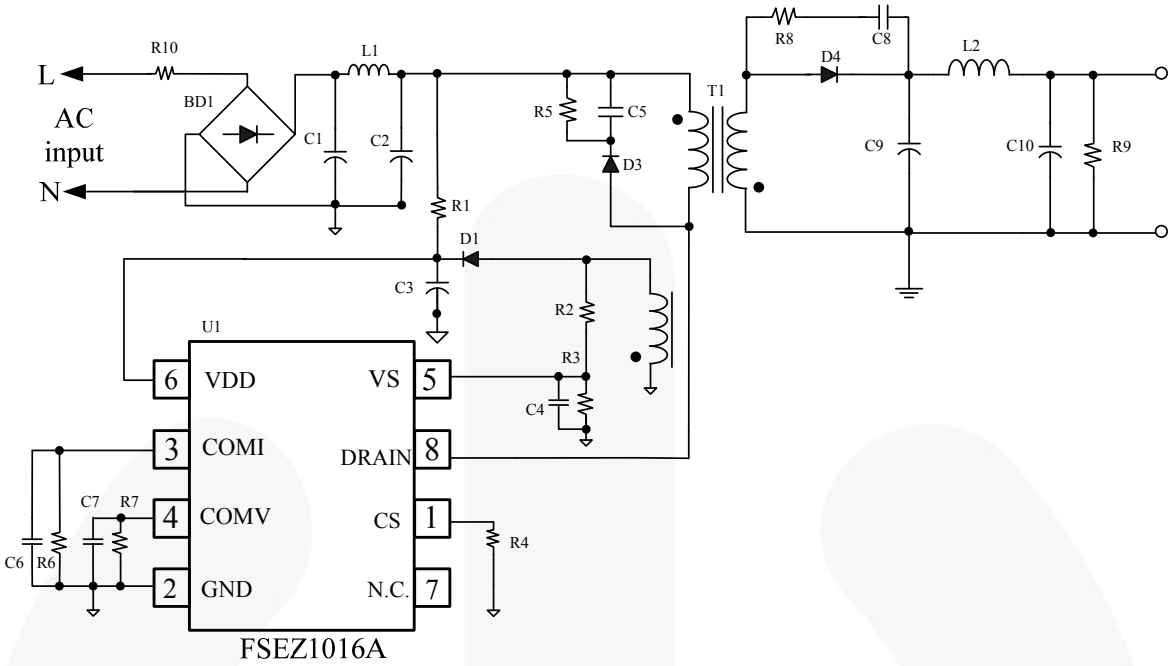

Figure 40. Application Circuit FSEZ1016A (FAN100 + MOSFET) (5V/1A)

BOM List

Symbol	Component	Symbol	Component
R1	Resistor 1.5MΩ	C1	Electrolytic Capacitor 1µF/400V
R2	Resistor 127KΩ 1%	C2	Electrolytic Capacitor 10µF/400V
R3	Resistor 20KΩ 1%	C3	Electrolytic Capacitor 10µF/50V
R4	Resistor 1.36Ω 1/2W 1%	C4	MLCC X7R 47pF
R5	Resistor 100KΩ 1/2W	C5	Snubber Capacitor 472pF/1KV
R6	Resistor 200KΩ	C6	MLCC X7R 683pF
R7	Resistor 39KΩ	C7	MLCC X7R 103pF
R8	Resistor 47Ω	C8	MLCC 102pF/100V
R9	Resistor 510Ω	C9	Electrolytic Capacitor 560µF/10V
R10	WireWound Resistor 18Ω	C10	Electrolytic Capacitor 330µF/10V
BD1	Rectifier Diode 1N4007 *4	L1	Inductor 1mH
D1	Diode 1A/200V FR103	L2	Inductor 5µH
D3	Diode 1A/1000V 1N4007	U1	FSEZ1016A
D4	Diode 5A/60V SB560	TR1	EE-16 Lm=1.5mH Pri:Sec:Aux=135:10:33

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Reference Circuits (Continued)

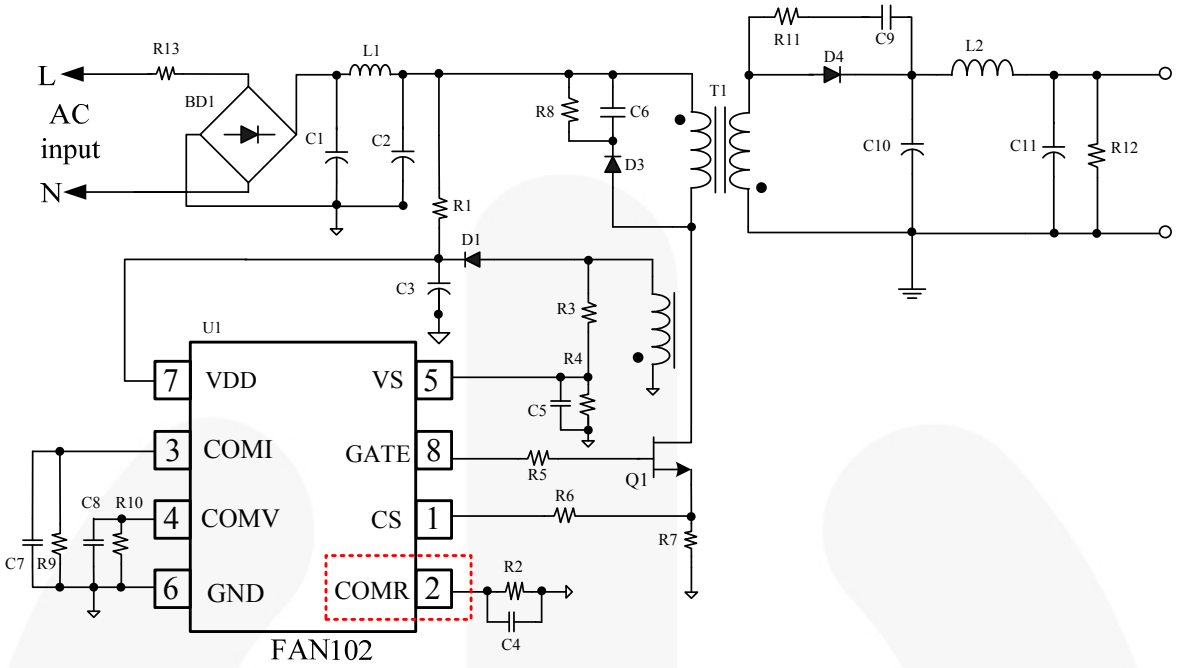

Figure 41. Application Circuit FAN102 (5V/1A)

BOM List

Symbol	Component	Symbol	Component	Symbol	Component
R1	Resistor 1.5MΩ 1/2 W	D3	Diode 1A/1000V 1N4007	Q1	1A/600V 1N60 TO-251
R2	Resistor 82KΩ 1%	D4	Diode 5A/60V SB560	TR1	EE-16 Lm=1.5mH Pri:Sec:Aux=135:10:33
R3	Resistor 110KΩ 1%	C1	Electrolytic Capacitor 1μF/400V	U1	FAN102
R4	Resistor 18KΩ 1%	C2	Electrolytic Capacitor 10μF/400V		
R5	Resistor 47Ω	C3	Electrolytic Capacitor 10μF/50V		
R6	Resistor 100Ω	C4	MLCC 104pF		
R7	Resistor 1.4Ω 1/4W 1%	C5	MLCC X7R 22pF		
R8	Resistor 100KΩ 1/2W	C6	Snubber Capacitor 472pF/1KV		
R9	Resistor 200KΩ	C7	MLCC X7R 683pF		
R10	Resistor 47KΩ	C8	MLCC X7R 103pF		
R11	Resistor 20Ω	C9	MLCC 102pF/100V		
R12	Resistor 510Ω	C10	Electrolytic Capacitor 560μF/10V L-ESR		
R13	WireWound Resistor 18Ω	C11	Electrolytic Capacitor 330μF/10V L-ESR		
BD1	Rectifier Diode 1N4007 *4	L1	Inductor 1mH 1/2W		
D1	Diode 1A/200V FR103	L2	Inductor 5μH		

Reference Circuits (Continued)

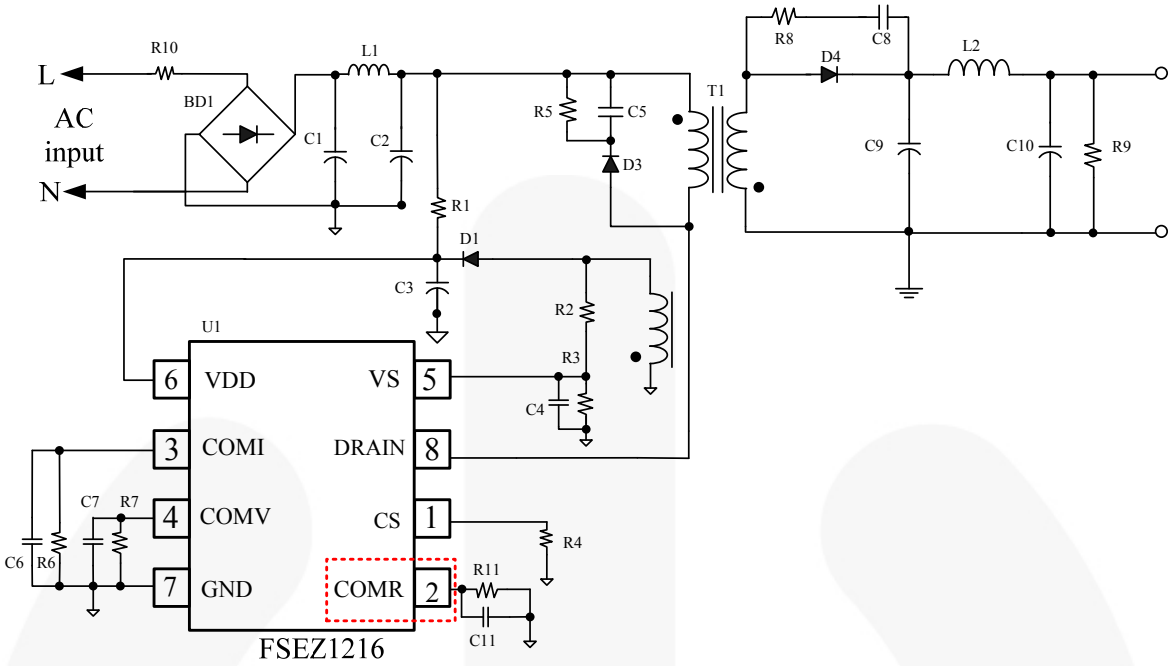

Figure 42. Application Circuit FSEZ1216 (5V/1A)

BOM List

Symbol	Component	Symbol	Component	Symbol	Component
R1	Resistor 1.5M Ω	D4	Diode 5A/60V SB560	U1	FSEZ1216
R2	Resistor 110KΩ 1%	C1	Electrolytic Capacitor 1μF/400V	TR1	EE-16 Lm=1.5mH Pri:Sec:Aux=135:10:33
R3	Resistor 18KΩ 1%	C2	Electrolytic Capacitor 10μF/400V		
R4	Resistor 1.4Ω 1/2W 1%	C3	Electrolytic Capacitor 10μF/50V		
R5	Resistor 100KΩ 1/2W	C4	MLCC X7R 47pF		
R6	Resistor 200KΩ	C5	Snubber Capacitor 472pF/1KV		
R7	Resistor 47KΩ	C6	MLCC X7R 683pF		
R8	Resistor 47Ω	C7	MLCC X7R 103pF		
R9	Resistor 510Ω	C8	MLCC 102pF/100V		
R10	WireWound Resistor 18Ω	C9	Electrolytic Capacitor 560μF/10V		
R11	Resistor 82KΩ 1%	C10	Electrolytic Capacitor 330μF/10V		
BD1	Rectifier Diode 1N4007 *4	C11	MLCC X7R 104pF		
D1	Diode 1A/200V FR103	L1	Inductor 1mH		
D3	Diode 1A/1000V 1N4007	L2	Inductor 5μH		

Related Datasheets

FAN100 — Primary-Side Regulation PWM Controller

FAN102 — Primary-Side Regulation PWM Controller

FSEZ1016A — Primary-Side Regulation PWM with Integrated Power MOSFET

FSEZ1216 — Primary-Side Regulation PWM with Integrated Power MOSFET

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